

Subst. Form PTO-1449 APPLICANT'S INFORMATION DISCLOSURE STATEMENT	Atty. Docket No.: END920000122US1 (EEN-10-5530)	Serial No.: To be assigned 10/657,483
	Applicant: Curcio et al	
	Filing Date: Herewith	Group: 1763

U.S. PATENT DOCUMENTS

Initial*		Document No.	Date	Name	Class	Subcl.	Filing Date
<i>See</i>	AA	3,795,047	03/05/74	Abolafia et al	29	625	06/15/72
	AB	5,092,032	03/03/92	Murakimi	29	830	05/15/91
	AC	5,135,606	08/04/92	Kato et al	156	631	12/07/90
	AD	5,200,026	04/06/93	Okabe	156	651	05/15/91
	AE	5,322,593	06/21/94	Hasegawa et al	156	633	11/20/92
	AF	5,624,268	04/29/97	Maeda et al	439	66	01/17/96
	AG	5,819,406	10/13/98	Yoshizawa et al	29	877	07/30/96
	AH	5,984,691	11/16/99	Brodsky et al	439	66	03/10/98
<i>See</i>	AI	6,059,579	05/09/00	Kresge et al	439	66	09/24/97
	AJ						
	AK						

FOREIGN PATENT DOCUMENTS

	Document No.	Date	Country	Class	Subcl.	Translation?
<i>See</i>	AL					
	AM					
	AN					

OTHER DOCUMENTS

<i>See</i>	AO	U.S. Application of Appelt et al for "Manufacturing Methods for Printed Circuit Boards and Printed Circuit Boards Made Thereby", Serial No. 08/968,988 (IBM Docket EN9-97-032)
<i>See</i>	AP	U.S. Application of Lauffer et al for "Composite Laminate Circuit Structure and Methods of Interconnecting the Same" (IBM Docket EN9-99-081)
<i>See</i>	AQ	IBM Technical Disclosure Bulletin, Vol. 37, No. 02A, "Improved and Cost-Reduced Interposer for Higher-Risk Processes", February, 1994
<i>See</i>	AR	"Multi Layer Substrate with Low Coefficient of Thermal Expansion", Kei Nakamura et al, 2000 International Symposium on Microelectronics, pp 235-240
	AS	
	AT	

Examiner: *Ala Chen*Date Considered: **9-30-05**

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if in conformance and not considered. If this form with next communication to applicant.